## REMARKS

Claims 1, 21, 40-41, and 44-46 have been amended. No claims have been cancelled. No claims have been added. Thus, claims 1-61 are pending.

Claims 44-45 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claims 44-45 have been amended as suggested by the Examiner. Claims 44-45 are now believed to be in compliance with 35 U.S.C. § 112, second paragraph. Accordingly, the rejection to claims 44-45 under 35 U.S.C. § 112, second paragraph should be withdrawn.

Claims 1-61 stand rejected as being anticipated by Holman (WO 99/30240). This rejection is respectfully traversed.

The present invention is directed to a memory bus system having improved electrical characteristics while being able to accommodate differing configurations of memory devices. Referring to Figs. 1-2, in the present invention a memory bus 28 is divided into a plurality of segments (e.g., segments 28a, 28b, and 28c) which are not directly coupled to each other. Memory modules, such as modules 24 and 26 may be inserted into the memory bus at the discontinuities between differing bus segments. More specifically, when a memory module 24, 26 is attached to the memory bus, an interface circuit 30 of the memory module serves to couple the two bus segments adjacent to the memory module. For example, in Fig. 1, interface circuit 30 of module 24 couples bus segment 28a to bus segment 28b. As can be seen in the Figs. 1-2, the memory bus 28 can be said to form a loop through the interface circuit 30 of the memory module. That is, data travels from one adjacent segment to another adjacent segment of the memory bus via an interface circuit 30 coupling the two adjacent segments.

Referring now also to Fig. 4, each memory module 24, 26 includes at least one memory device 54, 56, 58, 60 coupled to a second bus 32 which is internal to the memory module 24, 26. The interface circuit 30 is used to selectively transfer information between a memory module's second bus 32 and the memory bus 28 of the system. The interface circuit 30 may perform data reformatting, protocol conversion, and/or voltage conversion. That is, the interface circuit 30 electrically isolates the memory bus 28 from the internal bus 32 of a memory module, permitting differing numbers and types of memory modules to be attached to the memory bus 28 without adversely affecting the electrical characteristics of the memory bus 28. Similarly, this architecture permits the internal bus 32 of each memory module to be optimized for communication between the interface circuit 30 and the memory devices 54, 56, 58, 60 of the memory module 24, 26.

Accordingly, claims 1 and 21 as amended recite: "a first bus segment of a first data bus ...; a second bus segment of said first data bus, said second bus segment being separate and not connect to said first bus segment; ... an interface circuit ... said interface circuit being connected to said first data bus between said first and second bus segments of said first data bus for passing data through from said first bus segment to said second bus segment."

Similarly, claims 40-41 as amended recites: "a first data bus having at least first and second bus segments, said second bus segment being separate and not connect to said first bus segment; ... a data transfer interface circuit ... said interface circuit being connected to said first data bus between said first and second bus segments of said first data bus for passing data through from said first bus segment to said second bus segment."

Claim 42 recites "a bus system ... which loops through each of said interface devices;" while claims 43 recites "a bus which loops through ... at least one memory subsystem interface circuit."

Finally, claim 46 recites: "... passing data on said first data bus through from said first bus segment to said second bus segment and from said second bus segment to said first bus segment via said interface circuit."

Holman discloses a memory bus system in which memory modules are attached to the memory bus, and in which each memory module includes a data transfer circuits which "bridges" traffic between the memory bus and an internal memory module bus. The interface circuit is also capable of performing data format conversion, bus protocol conversion, and voltage conversion of signals between the two buses. However, as illustrated on, for example, Fig. 3, the system memory bus 323 of Holman is not comprised of discrete (i.e., not directly coupled) bus segments. While the Office Action is not wrong in identifying bus segments in the system memory bus 323, these segments are merely logical portions of the bus between attachment points of each memory controller 310, 316 of each memory module 306, 308. Each line 322, 324, 326, 328 of the system memory bus 323 is illustrated as a straight-through line from one end of the bus to another end. Thus, Holman cannot be said to teach or suggest the aforementioned limitations of the independent claims.

More specifically, with respect to claims 1, 21, 40, and 41, Holman fails to teach or suggest a memory bus comprised of a first and second segments which are not directly coupled to each other. Additionally, with respect to claims 42-43, Holman fails to teach or suggest looping a memory bus through an interface device or circuit of a memory module. Finally, with respect to claim 46, Holman fails to teach or suggest transferring information from one segment of the system memory bus 323 to another segment via a memory interface circuit or device. The depending claims are believed to be allowable for these reasons and because the combinations defined in the claims are not shown or suggested by the prior art of record.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: September 16, 2003

Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
Christopher S. Chow
Registration No.: 46,493
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant